# Constable: Improving Performance and Power Efficiency by Safely Eliminating Load Instruction Execution

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*Load instructions often limit instruction-level parallelism (ILP) in modern processors due to data and resource dependences they cause. Prior techniques like Load Value Prediction (LVP) and Memory Renaming (MRN) mitigate load data dependence by predicting the data value of a load instruction. However, they fail to mitigate load resource dependence as the predicted load instruction gets executed nonetheless (even on a correct prediction), which consumes hard-to-scale pipeline resources that otherwise could have been used to execute other load instructions.*

*Our goal in this work is to improve ILP by mitigating both load data dependence and resource dependence. To this end, we propose a purely-microarchitectural technique called* Constable*, that safely eliminates the execution of load instructions. Constable dynamically identifies load instructions that have repeatedly fetched the same data from the same load address. We call such loads* likely-stable. *For every likely-stable load, Constable (1) tracks modifications to its source architectural registers and memory location via lightweight hardware structures, and (2) eliminates the execution of subsequent instances of the load instruction until there is a write to its source register or a store or snoop request to its load address.*

*Our extensive evaluation using a wide variety of 90 workloads shows that Constable improves performance by* 5.1% *while reducing the core dynamic power consumption by* 3.4% *on average over a strong baseline system that implements MRN and other dynamic instruction optimizations (e.g., move and zero elimination, constant and branch folding). In presence of 2-way simultaneous multithreading (SMT), Constable's performance improvement increases to* 8.8% *over the baseline system. When combined with a state-of-the-art load value predictor (EVES), Constable provides an additional* 3.7% *and* 7.8% *average performance benefit over the load value predictor alone, in the baseline system without and with 2-way SMT, respectively.*

## 1. Introduction

Extracting high instruction-level parallelism (ILP) [66, 146] is essential for designing high-performance processors. However, ILP often gets limited by data dependence (i.e., the result of one instruction would be consumed by the other) and resource dependence (i.e., two or more instructions contending for the same limited hardware resource) between instructions [97, 137, 165, 176]. Load instructions are a major source of ILP limitation in modern workloads due to both data dependence and resource dependence [27]. On the one hand, a load instruction typically takes longer latency to execute than most non-memory instructions since a load performs two component operations: (1) compute the load address, and (2) fetch the data by accessing the memory hierarchy. As a result, the instructions that depend on the load instruction often

stall for multiple cycles, which can limit ILP. On the other hand, a load instruction consumes multiple hard-to-scale hardware resources (e.g., reservation station entry, port to address generation unit, L1-data cache read port) which often causes resource dependence in the pipeline, also limiting ILP.

Prior works propose many latency tolerance techniques to improve ILP by mitigating load data dependence. Load Value Prediction (LVP) [32, 42, 43, 71, 98, 107, 114, 139–143, 151, 153–155, 159, 160] and Memory Renaming (MRN) [120, 121, 147, 177, 178] are two such widely-studied techniques that mitigate load data dependence via data value speculation. LVP and MRN speculatively execute load-data-dependent instructions using the predicted value of the load instruction, thus improving ILP.

**Key limitation.** Even though LVP and MRN provide performance benefits by breaking load data dependence, the predicted load instruction still needs to be executed nonetheless to verify the speculated load value, which takes hard-to-scale hardware resources that otherwise could have been utilized for executing other load instructions. In other words, LVP and MRN provide performance benefits by mitigating load data dependence, but they *do not* mitigate load resource dependence, which leaves a significant performance and power consumption improvement opportunity on the table (see §4.4).

**Our goal** in this work is to improve ILP by mitigating *both* load data dependence and resource dependence. To this end, we propose a lightweight, purely-microarchitectural technique called **Constable**, which safely eliminates the entire execution of a load instruction (i.e., both load address computation and data fetch from memory hierarchy).

The **key insight** behind Constable is that a dynamic load instance $I_2$ of a static load instruction $I$ is bound to fetch the same value from the same memory location as the previous dynamic instance $I_1$ of the same static load instruction when the following two conditions are satisfied.

- **Condition 1**: None of the source registers of $I$ has been written between the occurrences of $I_1$ and $I_2$.
- **Condition 2**: No store or snoop request has arrived to the memory address of $I_1$ between the occurrences of $I_1$ and $I_2$.

Satisfying Condition 1 ensures that $I_2$ would have the same load address as $I_1$, and thus the address computation operation of $I_2$ can be safely eliminated. Satisfying Condition 2 ensures that $I_2$ would fetch the same value from the memory as $I_1$, and thus the data fetch operation of $I_2$ can be safely eliminated.

**Key mechanism.** Constable exploits this key insight to safely eliminate executing a load instruction while breaking load data dependence in two key steps. First, Constable dynamically identifies load instructions that have repeatedly fetched the same data value from the same load address. We call such

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loads *likely-stable.*[1] Second, when Constable gains enough confidence that a given load instruction is likely-stable, Constable tracks modifications to the source architectural registers the load instruction and its memory location via two small hardware structures. Constable eliminates the execution of all future instances of the likely-stable load and breaks the load data dependence using the last-fetched value of the load instruction, until there is a write to its source registers or a store or snoop request to its load address.

**Key results.** We evaluate Constable using a diverse set of *90* workloads (which includes all workloads from SPEC CPU 2017 [17] suite and many well-known `Client`, `Enterprise`, and `Server` workloads) over a strong 6-wide superscalar baseline processor that already implements Memory Renaming and various other dynamic instruction optimizations like zero elimination [68], move elimination [64,68], constant folding [64,68], and branch folding [60]. Our evaluation yields five key results that show Constable's effectiveness. First, Constable improves performance on average by (up to) $5.1\%$ ($31.2\%$) over the baseline, while reducing the core dynamic power consumption by $3.4\%$ ($24.6\%$). Second, when combined with a state-of-the-art value predictor (EVES [155]), Constable improves performance by $8.5\%$ on average over the baseline, which is $3.7\%$ more performance than EVES alone. Third, in a 2-way simultaneous multithreading [62] configuration, (a) Constable alone improves performance on average by $8.8\%$ over the baseline, and (b) Constable combined with EVES outperforms EVES alone by $7.8\%$ on average. Fourth, by eliminating both address computation and data fetch component of load execution, Constable reduces the reservation station allocations and L1-data cache accesses by $8.8\%$ and $26\%$, respectively, which results in dynamic power savings. Fifth, Constable's benefits come at a modest storage overhead of only 12.4 KB per core.

We make the following **key contributions** in this work:

- We show that a significant fraction (on average by $34.2\%$ and up to $68.3\%$) of all dynamic loads repeatedly *fetch the same value from the same memory address across the entire workload*. By analyzing the disassembly of fully-optimized workload binaries, we show that even a state-of-the-art compiler with full optimization often fails to optimize such load instructions at compile time due to various empirically-observed reasons, e.g., accessing runtime constants and accessing local variables in inlined functions (see §4.1).

- We show that *ideally* eliminating the execution of such load instructions while breaking their load data dependence has more than twice the performance headroom ($9.1\%$ on average) than breaking only load data dependence via *ideal* load value prediction ($4.3\%$ on average). This performance gap demonstrates the opportunity to improve ILP by mitigating load resource dependence (see §4.4).

- We propose Constable, a microarchitectural technique that dynamically identifies load instructions that repeatedly fetch the same data from the same address using a confidence-based mechanism and eliminates the execution of such instructions by tracking modifications to their source registers and store and snoop requests to their addresses (see §5).

- We propose a practical, lightweight microarchitecture for Constable that safely eliminates load execution in the presence of aggressive out-of-order load issue in modern multi-

core processors (see §6).

- We extensively verify the correctness of Constable by matching the outcome of every instruction in microarchitectural simulation with that in functional simulation over a large suite of 3400 traces (see §8.5).

- We show that Constable improves performance by $5.1\%$ on average (see §9.1.1) while reducing the core dynamic power consumption by $3.4\%$ (see §9.5) and incurring a modest storage overhead of only 12.4 KB over a strong superscalar processor that implements various dynamic instruction optimizations. Constable's benefits further increase in presence of simultaneous multithreading (see §9.1.2).

- We open-source a binary instrumentation tool that we use to identify load instructions that repeatedly fetch the same value from the same memory address in any off-the-self x86-64 binary in https://github.com/CMU-SAFARI/Load-Inspector (see §4.2).

## 2. Background

Extracting high instruction-level parallelism (ILP) [66,146] is essential in providing high single-thread and multi-thread performance in modern processors [80,94,172]. Unfortunately, ILP often gets limited by *data dependence* and *resource dependence* between instructions [27,97,137,165,176].[2] Data dependence limits ILP due to data flow (communications) between instructions, whereas resource dependence (also called structural dependence) limits ILP due to contention for limited hardware resources in the system (e.g., execution unit, load port).

Load instructions are a major source of ILP limitation in modern workloads due to both data and resource dependence [27]. Load instructions typically have longer latency than most non-memory instructions since they perform multiple component operations in a single instruction. Fig. 1 shows the two key component operations of a load instruction's execution in a traditional nine-stage out-of-order (OOO) processor pipeline [79,137]. The processor first computes the load address of an issued load instruction in the execute stage of the pipeline. The processor then fetches the data by accessing the memory hierarchy in the memory stage, which may require accessing the lower levels of memory hierarchy (e.g., the main memory). As a result, the dependents of a load instruction often stall for several cycles, thus significantly limiting ILP.
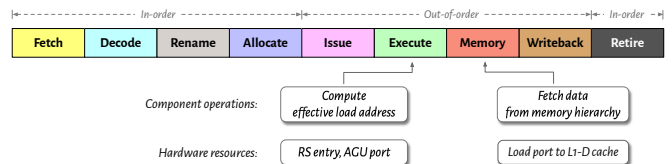


**Figure 1: Two component operations of a load instruction execution and their associated pipeline resources.**

A load instruction also uses several key hardware resources during its execution. As shown in Fig. 1, a load instruction consumes (1) a reservation station (RS) entry and an address generation unit (AGU) port to compute its load address, and (2) a load port to the L1-data (L1-D) cache to fetch the data from the memory hierarchy. Many of these hardware resources are hard to scale due to their non-trivial area and power overheads. As a result, a load instruction often causes resource dependence in the pipeline, thus limiting ILP.

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[1]Hence the name Constable, that *polices* the likely-stable loads to safely eliminate them.

[2]ILP also gets limited by frequent *control dependence* [137,138,176], which is outside the scope of this work.

Prior works propose many techniques to mitigate load data dependence by tolerating load instruction latency. *Load Value Prediction* and *Memory Renaming* are two such key techniques that mitigate load data dependence via speculative execution.

**Load Value Prediction (LVP)** [32, 42, 43, 71, 98, 107, 114, 139–143, 151, 153–155, 159, 160] breaks load data dependence by predicting the value of a load instruction and speculatively executing load-data-dependent instructions with the predicted value. The predicted value is later verified by executing the load instruction. A correct prediction increases ILP, but an incorrect prediction leads to re-execution of load-dependent instructions, incurring both performance and power overhead.

**Memory Renaming (MRN)** [120, 121, 147, 177, 178] learns the dependence relationship between a store-load instruction pair, and speculatively executes the load-dependent instructions by forwarding the data directly from the associated store instruction. The forwarded data is later verified by executing the load. A correct data forwarding increases ILP, whereas an incorrect forwarding incurs both performance and power overhead due to re-execution of load-dependent instructions.

## 3. Motivation and Goal

Even though LVP and MRN provide performance benefit by breaking load data dependence, the predicted load gets executed nonetheless to verify the speculated load value, which takes scarce and hard-to-scale hardware resources that otherwise could have been utilized for executing other load instructions. In other words, LVP and MRN provide performance benefits by mitigating load data dependence, but they *do not* mitigate load resource dependence.

To illustrate how LVP provides performance benefit by mitigating data dependence,[3] yet the benefit may get limited by resource dependence, Fig. 2(a) and (b) show the execution timeline of a code example in a processor without and with LVP, respectively. For simplicity, we assume that the OOO processor has fetch, issue, and retire bandwidth of two instructions, and one load execution unit (comprised of an AGU and a load port). We also assume a perfect LVP. As Fig. 2(a) shows, $I_1$ gets issued to the load execution unit in cycle-5, thus stalling $I_2$. In cycle-6, an older load instruction $I_x$ (not shown in the figure) becomes ready to execute and gets issued to the load execution unit, thus stalling $I_2$ even further. Stalls like these, where a load instruction gets delayed due to limited hardware resources (i.e., resource dependence), frequently occur in a modern high-performance processor with deeper and wider pipeline, as we quantitatively show in §4.3. These stalls get exacerbated further in the presence of performance-enhancement techniques like simultaneous multithreading (SMT) [62], where a hardware resource may get shared across SMT threads.

When LVP is employed, as shown in Fig. 2(b), both loads $I_1$ and $I_2$ get value-predicted and the data-dependent instruction $I_3$ retires 4 cycles earlier than in the processor without LVP. However, since both $I_1$ and $I_2$ need to get executed to verify their respective predicted values, $I_2$ still experiences stalls in cycle-5 and 6 due to resource dependence. If we can safely eliminate the execution of $I_1$ while breaking its data dependence, as shown in Fig. 2(c), we can enable $I_2$ to get issued to the load execution unit in cycle-5, which provides an

additional 2 cycles savings on top of the processor with LVP.[4]



Figure 2: Execution timeline of a code example in a processor (a) without a load value predictor (LVP), (b) with LVP, and (c) with LVP and load elimination.

We conclude that LVP and MRN may improve performance by mitigating load data dependence, but they leave performance improvement opportunity by not mitigating load resource dependence.

### 3.1. Our Goal

**Our goal** in this work is to improve ILP by mitigating *both* load data dependence and resource dependence. To this end, we propose a lightweight, purely-microarchitectural technique called *Constable*, which safely eliminates the entire execution of a load instruction (i.e., both load address computation and data fetch from memory hierarchy).

## 4. Performance Headroom of Constable

To understand the performance headroom of Constable, we first study the static load instructions that repeatedly fetch the same value from the same load address *across the entire workload trace*. We call such a load *global-stable*. Essentially, a global-stable load is a prime candidate for elimination since both load address computation and data fetch operations of its execution produce the same result across all dynamic instances of the instruction. We then quantify the resource dependence on global-stable loads (§4.3), and the performance benefit of ideally eliminating all global-stable load execution (§4.4).

### 4.1. Global-Stable Loads in Real Workloads

Intuitively, global-stable load instructions would be hard to find in real workloads since such instructions should already be optimized by the compiler. However, we observe that a significant fraction of load instructions in real workloads are global-stable even after aggressive compiler optimizations applied. Fig. 3 shows the fraction of dynamic load instructions that are global-stable on average across 90 workloads divided into five categories. §8 discusses our evaluation methodology. We make two key observations. First, 34.2% of all dynamic loads are global-stable. Second, the fraction of global-stable loads are much higher in `Client`, `Enterprise`, and `Server` workloads as compared to SPEC CPU 2017 workloads (i.e., `ISPEC17` and `FSPEC17` categories). We conclude that global-stable load instructions are relatively abundant in real workloads.

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[3]Since LVP and MRN work on conceptually similar principles, we use LVP for this discussion without loss of generality.

[4]Similarly, $I_2$ can potentially be eliminated as well, providing further savings in execution time (not shown in Fig. 2).
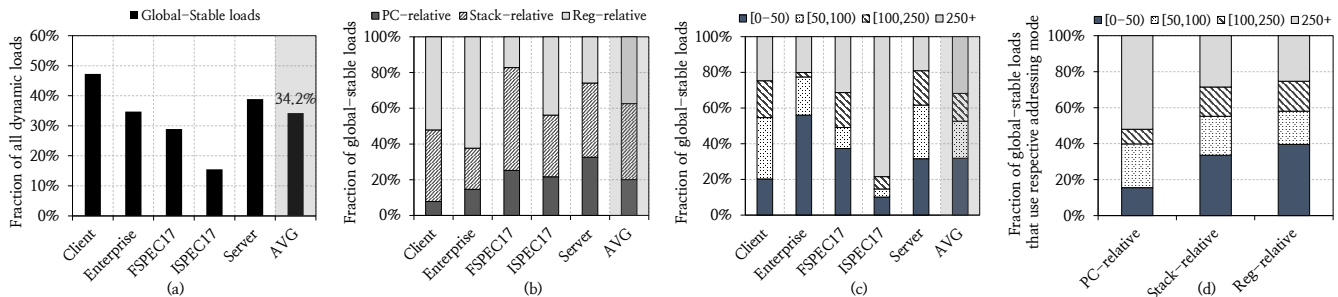
**Figure 3: (a) Fraction of dynamic loads that are global-stable. Distribution of global-stable loads by their (b) addressing mode and (b) inter-occurrence distance. (d) Distribution of inter-occurrence distance of global-stable loads from each addressing mode.**

#### 4.1.1. Characterization of Global-Stable Loads.
To understand the source of the global-stable loads in workloads (e.g., accessing variables in global scope, memory accesses in a tight loop), we further characterize these loads by their addressing mode and the inter-occurrence distance (i.e., the number of instructions between two successive dynamic instances of the same global-stable load instruction). Fig. 3(b) shows the breakdown of global-stable loads based on their addressing mode. The key takeaway is that global-stable loads use various different addressing modes. On average, 20%, 42.6%, and 37.4% of all global-stable loads use PC-relative (e.g., loads that access variables in the global scope), stack-relative (i.e., loads that access stack segment using RSP or RBP as their only source register), and register-relative (i.e., loads that use other general-purpose architectural registers as their source) addressing. Fig. 3(c) shows the breakdown of global-stable loads based on their inter-occurrence distance. The key takeaway is that global-stable loads have a bimodal inter-occurrence distance distribution. 31.9% of global-stable loads reoccur within 50 instructions (e.g., loads in a tight loop) on average, whereas 31.8% loads reoccur more than 250 instructions away (e.g., accessing a global-scope variable across function calls). Fig. 3(d) further shows the distribution of inter-occurrence distance of global-stable loads from each addressing mode. As we can see, global-stable loads that use PC-relative addressing have long inter-occurrence distance (52% of these loads have inter-occurrence distance of 250 or more instructions), whereas global-stable loads that use register-relative addressing have short inter-occurrence distance (39.6% of these loads have inter-occurrence distance of less than 50 instructions).

We conclude with three key takeaways. First, global-stable load instructions pose diverse characteristics, both in addressing mode and inter-occurrence distance. Second, the inter-occurrence distance of global-stable loads changes significantly depending on their addressing mode. Third, an effective load elimination technique should capture elimination opportunities across both short and long inter-occurrence distances.

### 4.2. Why Do Global-Stable Loads Exist?

To understand why a compiler with aggressive optimization fails to avoid global-stable load instructions, we use a custom-made binary instrumentation tool[5] to analyze the disassembly of workload binaries compiled with full optimization using a state-of-the-art off-the-shelf compiler. Fig. 5(a) and (b) show a code example from `541.leela_r` from SPEC CPU 2017 [17] benchmark suite and its disassembly, respectively. The work-

load is compiled using the latest GNU g++-13.2 compiler [5] at full optimization (i.e., using -O3 flag [6]) for x86-64 instruction set architecture to produce the most optimized binary. The highlighted load instruction in Fig. 5 fetches the object pointer `s_rng` from memory. Since `s_rng` gets initialized only once at the beginning of the workload, the pointer variable effectively acts as a runtime constant and thus the highlighted load instruction is global-stable. The compiler could not eliminate this load instruction since it cannot reserve an architectural register across the global scope of the program to be reused for accessing the `s_rng` pointer.

Fig. 5(c) and (d) show two more examples of global-stable load instructions in a code example from `557.xz_r` of SPEC CPU 2017 suite and its disassembly, compiled in the same way as the previous workload. Each highlighted load instruction accesses an argument variable to the function `rc_shift_low` that does not change during the function invocation. Since the function is repeatedly called using the same arguments from the same caller function throughout the workload trace, both the load instructions act as global-stable loads. However, as the function `rc_shift_low` gets *inlined* within the body of its caller function (not shown here), the compiler could not allocate architectural registers to store and reuse these variables due to register pressure [46].

We conclude that a state-of-the-art off-the-shelf compiler often fails to optimize global-stable loads due to various empirically-observed reasons, such as accessing runtime constants and local variables of inline functions, combined with a limited number of architectural registers.[6]

### 4.3. Resource Dependence on Global-Stable Loads
To quantify the loss of ILP due to resource dependence stemming from global-stable loads, we analyze the utilization of load ports. Other hardware resources that are used during a load execution (e.g., RS entry and AGU port) may also cause resource dependence, but we omit them here due to brevity. Fig. 6(a) shows the fraction of total execution cycles where at least one load port is utilized (we call such cycles *load-utilized*), in our baseline processor[7] augmented with a state-of-the-art load value predictor EVES [155]. As we can see, on average 32.7% of the total execution cycles are load-utilized. Fig. 6(b) further categorizes the load-utilized cycles of each workload category based on whether or not a global-stable load utilizes

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[5]We call this tool *Load Inspector*, which is freely available at https://github.com/CMU-SAFARI/Load-Inspector.

[6]We also observe that merely increasing the number of x86-64 architectural registers from 16 to 32 has negligible impact on eliminating the global-stable loads at compile time (see appendix B in the extended version [39]).

[7]Our baseline processor has an issue width of six instructions per cycle with three AGU and three load ports, which support a maximum throughput of three loads per cycle.
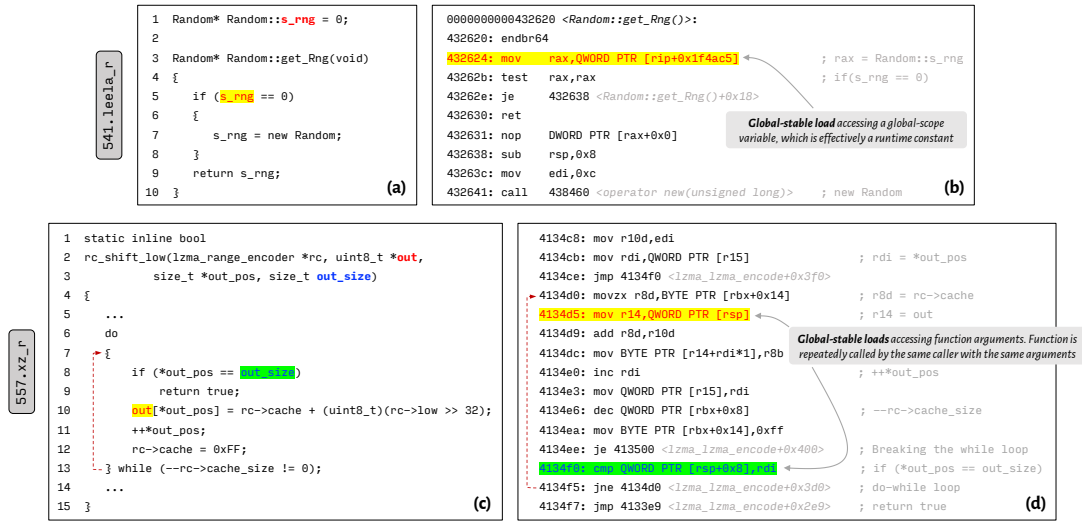
Figure 5: Code example and disassembly from `541.leela_r` and `557.xz_r` of SPEC CPU 2017 suite.

a load port. As we can see, for $23.0\%$ of all load-utilized cycles, a global-stable load takes a load port for its execution, while a non-global-stable load (i.e., a static load instruction that does not fetch the same value from the same load addresses across all dynamic instances) is waiting to be scheduled on the same port. Had the execution of global-stable loads be eliminated, the non-global-stable loads could have been scheduled faster, which in turn would provide performance benefit. Thus, we conclude that global-stable load instructions causes significant resource dependence, which can be mitigated by eliminating their execution altogether.
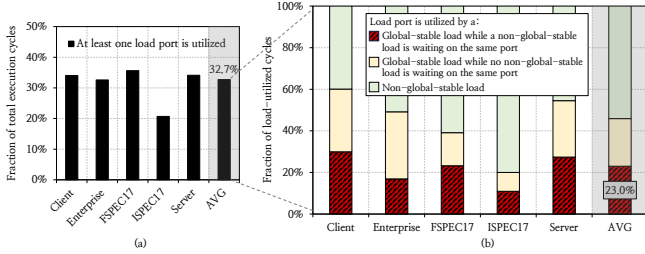


Figure 6: (a) Fraction of total execution cycles where at least one load port is utilized (we call such cycles *load-utilized*). (b) Categorization of load-utilized cycles based on whether or not a global-stable load utilizes a load port.

### 4.4. Performance Headroom

To measure the performance headroom of eliminating global-stable loads, we model an *Ideal Constable* configuration that identifies *all* global-stable load instructions offline and eliminates both component operations of their execution (i.e., load address computation and data fetch). We also compare Ideal Constable's performance against three other configurations: (1) *Ideal Stable LVP*, where *all global-stable* load instructions identified offline are perfectly value predicted, and they are are also executed to verify the predictions, (2) *Ideal Stable LVP with data fetch elimination*, where all global-stable load instructions are perfectly value predicted, and the value-predicted loads are executed only until the end of address generation, and (3) $2\times$ *load execution width* configuration, where the number of load execution units are doubled over the baseline. Fig. 7 shows the speedup of each configuration over baseline.
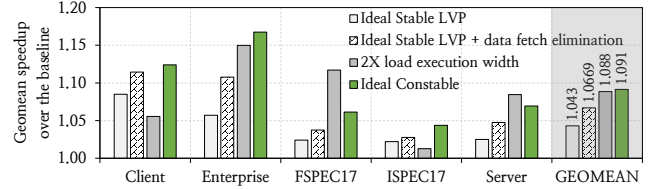


Figure 7: Speedup of Ideal Constable against Ideal Stable LVP and a processor with $2\times$ load execution width of the baseline.

We make four key observations from Fig. 7. First, Ideal Constable provides $9.1\%$ performance improvement on average over the baseline. This shows that eliminating the execution of global-stable loads has high performance headroom. Second, Ideal Constable significantly outperforms Ideal Stable LVP ($4.3\%$ on average). This shows that mitigating both data and resource dependence (as done by Ideal Constable) has higher performance potential than only mitigating data dependence (as done by Ideal Stable LVP). Third, Ideal Stable LVP with data fetch elimination outperforms Ideal Stable LVP ($6.7\%$ on average), yet it falls short to the Ideal Constable. This shows that eliminating *both* the address computation and data fetch operations of a load execution has higher performance potential than just eliminating the data fetch. Fourth, Ideal Constable even slightly outperforms $2\times$ load execution width configuration, which incurs significantly higher area and power overhead. We conclude that Constable has significant potential performance benefit by mitigating *both* load data and resource dependence.

## 5. Constable: Key Insight

Constable is based on the **key insight** that a dynamic instance $I_2$ of a static load instruction $I$ is bound to fetch the same value from the same memory location as the previous dynamic instance $I_1$ of the same static load instruction if the following two conditions are satisfied:

- **Condition 1**: None of the source registers of $I$ has been written between the occurrences of $I_1$ and $I_2$.
- **Condition 2**: No store or snoop request has arrived to the memory address of $I_1$ between the occurrences of $I_1$ and $I_2$.

Satisfying Condition 1 ensures that $I_2$ would have the same load address as $I_1$, and thus the address computation operation of $I_2$ can be safely eliminated. Satisfying Condition 2 ensures

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that $I_2$ would fetch the same value from the memory as $I_1$, and thus the data fetch operation of $I_2$ can be safely eliminated.

Constable exploits this observation to operate in two key steps. First, Constable dynamically identifies load instructions that have repeatedly fetched the same value from the same load address. We call such loads *likely-stable.* Second, when Constable gains enough confidence that a given load instruction is likely-stable, Constable tracks modifications to the source architectural registers of the load instruction and its memory location via two small hardware structures. Constable eliminates the execution of all future instances of the likely-stable load and breaks the load data dependence using the last-fetched value - until there is a write to the source registers or a store or snoop request to the load address.

## 6. Constable: Microarchitecture Design

### 6.1. Design Overview

Fig. 8 shows a high-level overview of Constable. Constable is comprised of three main hardware structures:

**Stable Load Detector (SLD).** SLD is a program counter (PC)-indexed table that serves three key purposes. First, SLD identifies whether or not a given load instruction is likely-stable by analyzing its past dynamic instances. Second, SLD decides whether or not the execution of a load instruction can be eliminated. Third, SLD provides the last-computed load address and the last-fetched data of a given likely-stable load instruction.

**Register Monitor Table (RMT).** RMT is an architectural-register-indexed table whose key purpose is to monitor modifications to architectural registers and avoid eliminating a load instruction when its source architectural register gets modified. Each RMT entry stores a list of load PCs that are currently getting eliminated that use the corresponding architectural register as their source. In the rename stage, every instruction looks up RMT using its destination architectural register and resets the elimination status of any load PC from the corresponding RMT entry in SLD to ensure that any future instances of that load instruction will not be eliminated. In essence, RMT enforces the Condition 1 for eliminating a load instruction (§5).

**Address Monitor Table (AMT).** AMT is a physical-address-indexed table whose key purpose is to monitor modifications in the memory and avoid eliminating a load instruction when the memory location from which it fetches the data gets modified. Each AMT entry stores a list of load PCs that are currently getting eliminated that access the corresponding physical memory address. Every store or snoop request looks up AMT using its physical address and resets the elimination status of any load PC from the corresponding AMT entry in SLD to ensure that any subsequent instances of that load will not be eliminated further. In essence, AMT enforces the Condition 2 for eliminating a load instruction (§5).

### 6.2. Identifying Likely-Stable Loads

SLD employs a confidence-based learning mechanism to identify likely-stable load instructions based on the execution outcomes of their past dynamic instances. Each SLD entry stores four key pieces of information: (1) last-computed load address, (2) last-fetched value, (3) a 5-bit *stability confidence level* and (4) a `can_eliminate` flag that represents whether or not an instance of this load instruction can be eliminated. When a non-eliminated load instruction completes execution in the writeback stage, Constable checks the SLD using the load PC
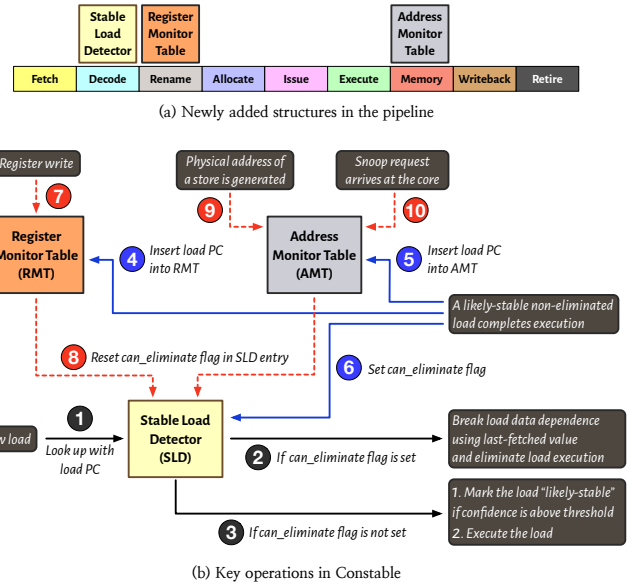


(a) Newly added structures in the pipeline



(b) Key operations in Constable

**Figure 8: Overview of Constable.**

to compare the last-computed load address and last-fetched value with the current load address and value. If both the address and value match, Constable increments the stability confidence level by one; otherwise, it halves the confidence. If the stability confidence level surpasses a threshold (set to 30 in our evaluation), Constable identifies subsequent load instances from the same PC as likely-stable.

### 6.3. Eliminating Load Execution

During the rename stage, a load instruction first checks the SLD using the load PC (❶ in Fig. 8). If the `can_eliminate` flag is set in the corresponding SLD entry, Constable breaks the load data dependence using the last-fetched value stored in the SLD entry and eliminates its execution (❷). If the `can_eliminate` flag is not set, Constable checks the stability confidence level stored in the SLD entry. If the confidence level is above threshold, Constable marks the load instruction as likely-stable and executes it normally as the baseline (❸). Only a load instruction marked as likely-stable can set the `can_eliminate` flag during the writeback stage of its execution (see §6.4.1).

**Microarchitecture for breaking load data dependence.** Breaking load data dependence requires supplying the load value to all dependent in-flight instructions. Prior works on LVP achieve this by writing the value to the physical register file (PRF) or to a separate value table [159]. Since writing to PRF either requires adding expensive write ports to PRF [134, 141, 143] or a latency-sensitive arbitration of the existing write ports [139, 159], Constable implements load data dependence breaking using a small extra register file (only 32 entries), called xPRF, which is dedicated to hold the values of the in-flight eliminated load instructions.[8]

If SLD decides to eliminate the load execution, Constable stores the last-fetched value provided by SLD in an available

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[8]We implement Constable using xPRF as having a small PRF to break data dependence has been shown to be more area- and energy-efficient than adding new write ports to the existing PRF [159]. However, Constable can also be implemented by adding or arbitrating PRF write ports. For a fair evaluation, we also implement the LVP and MRN techniques considered in this work using xPRF. As such, xPRF is not considered as an additional structure for Constable.

xPRF register and converts the load instruction into a three-operand register move instruction: the source is the xPRF register, the destination is the destination architectural register of the load, and the third operand is the last-computed load address provided by the SLD. If there is no available xPRF register, Constable does not eliminate the load and executes it normally as the baseline. We observe this happens rarely (only in $0.2\%$ of the instances) in our evaluation with a 32-entry xPRF. In the rename stage, the converted register move instruction simply maps its destination register to the source xPRF register to complete its execution (similar to move elimination [64,68]). Doing so enables the dependents of the converted register move instruction to get scheduled by reading the xPRF register value. In the allocation stage, the converted register move instruction allocates a reorder buffer (ROB) entry and a load buffer (LB) entry. The address field in the LB entry gets updated with the last-computed load address embedded within the move instruction as the third operand. This address field in the LB entry is later required to correctly disambiguate the eliminated load from the in-flight stores [70] as discussed in §6.5. Since the execution of the converted register move instruction has already been completed in the rename stage, the instruction bypasses the remaining pipeline stages and resources directly to retirement based on the in-order retirement logic.

## 6.4. Updating Constable Structures

### 6.4.1. Updates When a Likely-Stable Non-Eliminated Load Finishes Execution.
During the writeback stage of the pipeline, when a likely-stable yet not eliminated load finishes its execution, Constable updates its structures to eliminate subsequent instances of the same load instruction. This happens in three steps. First, Constable looks up RMT with its source architectural registers. For each source register, Constable inserts the load PC into the corresponding RMT entry (④). Second, Constable looks up AMT with the physical address of the load instruction. If the load address is found, Constable inserts the load PC into the corresponding AMT entry (⑤). If the address is not found, Constable inserts a new AMT entry for the load address and inserts the load PC into the new AMT entry. Third, Constable looks up SLD with the load PC and sets the `can_eliminate` flag of the corresponding entry (⑥). Setting the `can_eliminate` flag allows Constable to eliminate the execution of subsequent instances of the same load instruction.

### 6.4.2. Updates during Register Renaming.
In the rename stage, Constable checks the destination architectural register of every instruction and updates its structures to avoid eliminating subsequent instances of any load instruction that uses the destination register as its source. This happens in two steps. First, Constable looks up RMT with the architectural destination register of every instruction (⑦). If there is any load PC in the corresponding RMT entry, Constable looks up the SLD using each load PC and resets the `can_eliminate` flag in the corresponding entry in SLD (⑧).

### 6.4.3. Updates on a Store Instruction.
When the address of a store instruction gets generated, Constable updates its structures to avoid eliminating subsequent instances of any load instruction that fetches data from the same memory address as the store. This happens in two steps. First, Constable looks up AMT using the physical store address (⑨). If the address is found in AMT, Constable looks up SLD using each load PC in the AMT entry and resets the `can_eliminate` flag

from the corresponding entry in SLD (⑧). Second, after resetting `can_eliminate` flag for all load PCs in the AMT entry, Constable evicts the AMT entry.

### 6.4.4. Updates on a Snoop Request.
To safely eliminate loads in multi-core systems, Constable monitors snoop requests coming to the core and updates its structures to avoid eliminating subsequent instances of any load instruction that fetches data from the same memory address as the snoop. Constable handles a snoop request in a similar way as a store request. When a snoop request arrives at the core, Constable looks up AMT using the snoop address (⑩). If the address is found, Constable looks up SLD using each load PC in the AMT entry and resets the `can_eliminate` flag from the corresponding entry in SLD (⑧). Finally, Constable evicts the AMT entry.

## 6.5. Disambiguating Eliminated Loads from In-Flight Stores

When a store instruction computes its address, Constable accesses AMT and resets the `can_eliminate` flag for all load instructions accessing the same memory location (see §6.4.3). This prevents Constable from eliminating any *subsequent occurrences* of those load instructions. However, in a processor that aggressively issues loads out-of-order [67,70,119], there may be eliminated loads in the pipeline that are younger than the store instruction and whose addresses match with the store address. We observe that this happens rarely (see appendix A.2 in the extended version [39]) since Constable considers a load instruction to be eligible for elimination only if it meets the stability confidence level threshold. In such infrequent cases, Constable exploits the existing memory disambiguation logic [48,70] that matches the store address with the address of every load in the LB. If a violation is caught, Constable flushes the pipeline and re-executes all younger instructions, including the incorrectly-eliminated load (see the example in §6.8).

## 6.6. Maintaining Coherence in Multi-Core Systems

Constable relies on monitoring snoop requests for tracking modifications in the memory by other processor cores to safely eliminate loads in a multi-core system. However, monitoring snoop requests poses the following two key challenges.

**Loss of elimination opportunity due to clean eviction.** In a multi-core system with a directory-based coherence protocol [45], when a cacheline gets evicted from a core-private cache, the core-valid bit (CV-bit) corresponding that core (i.e., the *own core*) gets reset in the directory entry of that cacheline [22,23,74,152]. Since resetting CV-bit prevents the directory from sending any further snoop request to that cacheline to the core, on every core-private cache eviction, Constable needs to avoid eliminating any load instruction that accesses the evicted cacheline. This poses two key drawbacks. First, if the evicted cacheline is clean (e.g., eviction due to limited cache capacity or cache conflict), Constable loses elimination opportunity (we quantify the impact of such elimination opportunity loss in appendix A.3 in [39]). Second, for every core-private cache eviction, Constable needs to look up and invalidate the corresponding AMT entry, which increases design complexity. To address these drawbacks, we propose to *pin* the own core's CV-bit of a cacheline that is accessed by an eliminated load instruction. When the memory request of a likely-stable yet not eliminated load returns from the cache hierarchy, Constable pins the own core's CV-bit in the directory entry of that

cacheline. Pinning CV-bit ensures that (1) the coherence protocol would send any snoop request to that cacheline to the own core, even if the cacheline gets clean-evicted from the core-private cache, and (2) Constable does not need to look up AMT on every core-private cache eviction. The CV-bit is reset as soon as a snoop request is delivered to the core, as per the normal directory-based coherence protocol.

**Tracking snoop requests at cacheline address granularity.** Unlike a store instruction that contains a full memory address, a snoop request contains a cacheline address. Thus, to support AMT lookup using a snoop address, Constable indexes AMT using physical addresses at cacheline granularity. This may cause loss of elimination opportunities due to false address collisions (e.g., a store to a cacheline may reset the `can_eliminate` flag of a load instruction that accesses different bytes of the same cacheline accessed by the store). However, we find that the performance impact of such elimination opportunity loss is negligible. Constable with a cacheline-address-indexed AMT has only $0.4\%$ lower average performance than a Constable with full-address-indexed AMT. This is primarily because the compiler tends to lay out memory addresses accessed by likely-stable load instructions together (e.g., a group of function arguments laid out in the same cacheline of stack memory segment), which reduces the overhead of false address collisions.

## 6.7. Other Design Decisions

### 6.7.1. Architecting SLD.
Designing SLD with sufficient read/write ports is crucial for realizing Constable's performance benefits. Constable reads SLD for every load instruction to identify likely-stable loads in the rename stage (❶ in Fig. 8). Thus SLD needs to support the read bandwidth of the expected number of load instructions in a group of instructions getting renamed together in every cycle (we call this a *rename group*).[9] We observe that a rename group contains $1.93$ loads on average across all workloads, and $98.3\%$ of all rename groups have less than or equal to two loads. Thus, we model SLD with three read ports. If there are more than three loads in a rename group, we stall the rename stage until Constable finishes SLD lookup for every load in that group.

Constable may need to update the `can_eliminate` flag in SLD on every RMT update, which happens for each instruction in a rename group (❼ and ❽). Since each RMT entry may contain a list of likely-stable load PCs, the expected number of SLD updates per cycle can vary in a large range. Fig. 9(a) shows the average number of observed SLD updates per cycle for every workload as a box-and-whiskers plot.[10] As we can see, we observe only $0.28$ SLD updates per cycle on average across all workloads. $98.23\%$ of all cycles on average across all workloads have two or fewer SLD updates. This is because, at any point in time, only a small fraction of all load PCs ($14.7\%$ on average) satisfies the stability confidence level threshold in order to be tracked by RMT entries. Thus, we model SLD with two write ports. If there are more than two SLD updates in a cycle, we stall the rename stage until Constable finishes SLD update for every load instruction in that rename group.

### 6.7.2. Handling Wrong Path Execution.
In presence of branch prediction, Constable's structures may get updated

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[9]We model a six-wide rename architecture (see §8.1).

[10]Each box is lower- (upper-) bounded by the first (third) quartile. The box size represents the inter-quartile range (IQR). The whiskers extend to 1.5×IQR range on each side, and the cross-marked values in the box show the mean.
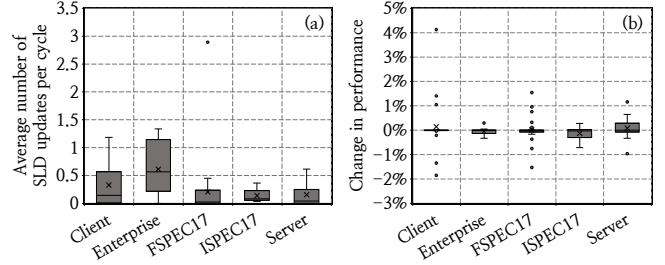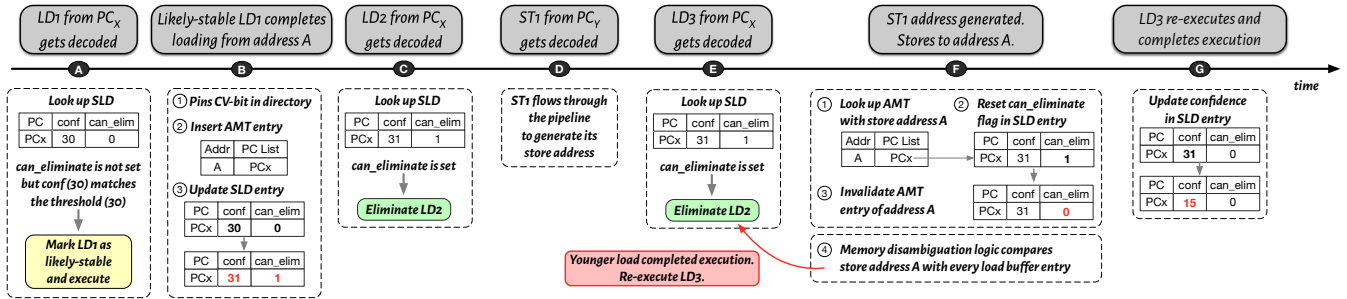


**Figure 9: (a) Average number of SLD updates per cycle during rename stage. (b) Change in performance when Constable's structures are updated only by correct path instructions vs. all instructions without updating Constable's structures on branch misprediction recovery.**

by wrong path instructions (especially, steps ❼ and ❽ in Fig. 8). This may result in an unnecessary loss of elimination opportunity, unless the structures are restored on a branch misprediction recovery. To understand the need for restoring Constable's structures, we measure the change in performance of Constable when its structures are updated only by the instructions on the correct path against when they are updated by all instructions without an update mechanism on branch misprediction recovery, and show it as a box-and-whiskers plot in Fig. 9(b). The key observation is that 82 out of 90 workloads show less than $1\%$ absolute change in performance, while the average performance change is only $0.2\%$. Thus, we model Constable without any update mechanism for its structures on a branch misprediction recovery.

### 6.7.3. Handling Changes in Physical Address Mapping.
AMT monitors memory locations accessed by all eliminated load instructions in physical address space. This poses a challenge: when the physical memory mapping changes, the physical memory address tracked by an AMT entry may not be associated with the corresponding eliminated load anymore. In that case, to avoid incorrectly eliminating load execution, Constable resets the `can_eliminate` flag of all SLD entries and invalidates all RMT and AMT entries when the physical memory mapping changes (e.g., context switch).

## 6.8. An Illustrative Example

To put it together, Fig. 10 illustrates an example of Constable's operation. For this example, we consider that the loads $LD_1$, $LD_2$, and $LD_3$ are three dynamic instances of the static load instruction $LD$ with a PC value $PC_x$ and the source registers of $LD$ do not get modified between $LD_1$ and $LD_3$. We also assume the stability confidence level threshold is set to 30.

When $LD_1$ gets decoded (Ⓐ in Fig. 10), Constable checks SLD and finds that the stability confidence level of $PC_x$ matches the threshold, yet the `can_eliminate` flag is not set. In this case, Constable marks $LD_1$ as likely-stable and executes it normally. When $LD_1$ finishes its execution (Ⓑ), Constable (1) pins the CV-bit corresponding to the own core in the coherence directory entry of address A, (2) updates AMT and RMT (not shown here), and (3) increments the stability confidence level in SLD. Since $LD_1$ is marked as likely-stable, Constable sets the `can_eliminate` flag in SLD entry. When $LD_2$ gets decoded (Ⓒ), Constable eliminates executing $LD_2$ since the `can_eliminate` flag is set. Now a store $ST_1$ from a different $PC_y$ gets decoded (Ⓓ). This store instruction would ultimately modify the memory address touched by $LD$.

Figure 10 content:

**A** — LD1 from PCx gets decoded
**B** — Likely-stable LD1 completes loading from address A
**C** — LD2 from PCx gets decoded
**D** — ST1 from PCy gets decoded
**E** — LD3 from PCx gets decoded
**F** — ST1 address generated. Stores to address A.
**G** — LD3 re-executes and completes execution

time →

**A — Look up SLD**

| PC | conf | can_elim |
|---|---|---|
| PCx | 30 | 0 |

*can_eliminate is not set but conf (30) matches the threshold (30)*

**Mark LD1 as likely-stable and execute**

**B —**
① Pins CV-bit in directory
② Insert AMT entry

| Addr | PC List |
|---|---|
| A | PCx |

③ Update SLD entry

| PC | conf | can_elim |
|---|---|---|
| PCx | 30 | 0 |

| PC | conf | can_elim |
|---|---|---|
| PCx | 31 | 1 |

**C — Look up SLD**

| PC | conf | can_elim |
|---|---|---|
| PCx | 31 | 1 |

*can_eliminate is set*

**Eliminate LD2**

**D —** ST1 flows through the pipeline to generate its store address

**E — Look up SLD**

| PC | conf | can_elim |
|---|---|---|
| PCx | 31 | 1 |

*can_eliminate is set*

**Eliminate LD2**

*Younger load completed execution. Re-execute LD3.*

**F —**
① Look up AMT with store address A

| Addr | PC List |
|---|---|
| A | PCx |

② Reset can_eliminate flag in SLD entry

| PC | conf | can_elim |
|---|---|---|
| PCx | 31 | 1 |

③ Invalidate AMT entry of address A

| PC | conf | can_elim |
|---|---|---|
| PCx | 31 | 0 |

④ Memory disambiguation logic compares store address A with every load buffer entry

**G — Update confidence in SLD entry**

| PC | conf | can_elim |
|---|---|---|
| PCx | 31 | 0 |

| PC | conf | can_elim |
|---|---|---|
| PCx | 15 | 0 |

Figure 10: An illustrative example of Constable's operation.

However, before $ST_1$ could generate its store address, $LD_3$, which is younger than $ST_1$ in program order, gets decoded (**E**) and Constable *incorrectly* eliminates its execution since the can_eliminate flag is set. When $ST_1$ finally generates its store address (**F**), Constable resets the can_eliminate flag to prevent eliminating subsequent instances of $LD$ and evicts the AMT entry. However, the existing memory disambiguation logic probes the load buffer with the store address and finds out that a younger load $LD_3$ has been incorrectly completed. As a result, the memory disambiguation logic aborts and re-executes $LD_3$ (and all instructions younger than $LD_3$ that are not shown here). When $LD_3$ completes its execution (**G**), it halves the stability confidence level counter.

## 6.9. Storage Overhead

Table 1 shows the storage overhead of Constable. Constable requires only 12.4 KB storage per core of the processor (see §8.1).

**Table 1: Storage overhead of Constable.**
(Our baseline system models a 48-bit physical address space)

| Structure | Description | Size |
|---|---|---|
| SLD | • # entries: 512 (32 sets × 16 ways)<br>• Entry size: tag (24b) + addr (32b) + val (64b) + confidence level (5b) + can_eliminate flag (1b) | 7.9 KB |
| RMT | • 16 load PCs for each stack registers (RSP and RBP)<br>• 8 load PCs for each remaining 14 architectural registers in x86-64 | 0.4 KB |
| AMT | • # entries: 256 (32 sets × 8 ways)<br>• Entry size: physical address tag (32b) + # hashed load PCs (4 × 24b) | 4.0 KB |
| Total | | 12.4 KB |

## 7. Differences from Related Prior Works

The key idea of early-executing the address computation and/or eliminating the data fetch operations of a load instruction has been explored in many prior works. We divide such works into the following four categories to better understand Constable's differences from them.

**Prior works that early execute address computation.** Prior works propose speculative and non-speculative techniques to early or fast execute address computation of a load instruction. [26] uses a fast, speculative carry-free addition to speed up load address computation. [27] caches the values of recently-used registers to speculatively compute load address. Early load address resolution (ELAR) [34] tracks stack register values using a small computation unit in the decode stage to *safely and non-speculatively* compute the load address of most stack loads immediately after the decode stage. Register file prefetching (RFP) [164] predicts the load address of an instruction to prefetch its data to the register file.

Constable differs from these works in one major way. These prior works necessitate the execution of the load instruction whose load address has been computed early. Works that *speculatively* compute load address [26, 27, 164] need to execute the load to verify the speculation. ELAR, which employs a safe technique to *non-speculatively* compute address of stack loads, still needs to fetch the load data from the memory hierarchy. Constable safely eliminates *both the address computation and the data fetch operations* of a load execution altogether. We evaluate Constable against ELAR and RFP in §9.2 demonstrating its performance benefits.

**Prior work that eliminates the data fetch operation.** Lipasti et al. (we call it the Lipasti load value predictor [108] or LLVP) observe that some static load instructions have highly-predictable load values, which they call *constant loads*. LLVP proposes a microarchitecture to bypass the data fetch operations of constant loads. LLVP maintains addresses of constant loads in a table called constant verification unit (CVU) and invalidates a CVU entry by observing a store request to the corresponding address. To verify the predicted value of a constant load, LLVP first computes its load address. If the address is found in CVU, LLVP bypasses the data fetch operation.

Constable differs from LLVP in one major way. LLVP advocates for eliminating *only* the data fetch operation of a value-predicted constant load. Constable, on the other hand, eliminates both the address computation and data fetch operations of a load instruction execution. As §4.4 shows, eliminating both address computation and data fetch operations (as done by Ideal Constable) provides higher performance benefit than eliminating only data fetch (as done by Ideal Stable LVP with data fetch elimination).

**Prior works that enable memoization.** Memoization [116], caches computed results from repeated code executions, enabling a program or a microarchitecture to skip redundant computations when encountering identical input sets. Memoization has been applied in both software [58, 116, 148, 173, 174] and in hardware at various program granularities, including instruction-level [53, 76, 117, 149, 166, 167], basic-block-level [83], trace-level [73], and function-level [54]. Early works on instruction-level memoization aim to accelerate long-latency operations (e.g., floating point multiplication and division) by storing their operands and results in value caches [133, 149]. Sodani and Sohi propose a PC-indexed *reuse buffer* to store the results of (multiple) dynamic instances of every static instruction [166]. Molina et al. improve upon the reuse buffer to capture reuse of results across dynamic instances of different static instructions [117].

Constable, in principle, resembles instruction-level memoization with three key differences that make Constable more per-

formant, lightweight, and usable in today's high-performance multi-core processors. First, prior works aim to memoize (multiple) results of *every* static instruction, irrespective of whether or not the results would be useful for instruction elimination. This requires a large memoization buffer, often as large as L1 data cache [52, 186, 187], to capture elimination opportunities across long inter-occurrence distances (see §4.1.1). Gonzalez et al. have shown that, while such a large memoization buffer may provide a significant performance benefit, the benefits reduce significantly when the latency to access the buffer is considered [72]. Constable on the other hand (a) only targets loads, and (b) employs a confidence-based mechanism to filter out likely-stable load instructions from all loads. This significantly reduces Constable's storage overhead and design complexity (e.g., port requirements of SLD as discussed in §6.7.1) while providing high elimination coverage. Second, prior works may delay retrieving the memoized instruction output until its source register values are available [53, 76, 117, 149]. As a result, these works may not alleviate resource dependence on hardware structures like the reservation station. Constable, however, explicitly monitors changes in source architectural registers of likely-stable load instructions and eliminates them early in the pipeline, alleviating resource dependence from both load reservation station and load execution unit. Third, prior works may not be applied in today's high-performance multi-core processors as they do not address challenges related to (a) keeping memoization buffer coherent across multiple cores, and (b) maintaining program correctness in presence of out-of-order load issue. Constable addresses both these challenges (§6.5 and §6.6) and we extensively verify its correctness via functional simulation (§8.5).

**Prior works on dynamic instruction optimization.** Prior works on trace-cache-based optimizations [68, 86] and rePLay framework [63, 136] enable a wide range of runtime code optimizations (e.g., move elimination, zero-idiom elimination) that can eliminate instructions in microarchitecture. Continuous optimization (CO) [64] builds on these works and enables removing redundant instructions (including loads) using the register renaming logic.

Constable differs from these works in two key ways. First, these schemes learn optimizations offline per-trace (or frame) basis. Constable learns optimization online and applies directly to the program's dynamic instruction stream. Second, unlike Constable, CO does not eliminate a load instruction in a multi-core system in order to maintain the coherency. Our baseline system already implements many runtime optimizations to non-memory instructions at renaming stage (see §8).

## 8. Methodology

### 8.1. Performance Modeling

We evaluate Constable using an in-house, cycle-accurate, industry-grade simulator that simultaneously runs both functional and microarchitectural simulation on a workload. We faithfully model a 6-wide out-of-order processor core configured similar to the Intel Golden Cove [7,8,10,15] as our baseline. Table 2 shows the key microarchitectural parameters. We include MRN and various dynamic optimizations in the rename stage of the baseline processor, as highlighted in bold. For a comprehensive analysis, we evaluate Constable and other competing mechanisms on the baseline system, both without SMT (called *noSMT*) and with 2-way SMT (called *SMT2*). For

noSMT configuration, all hardware resources inside core are fully available to the single running software context. For SMT2 configuration, resources inside core (including Constable) are either statically-partitioned or dynamically-shared between both software contexts [55]. Unless stated otherwise, all reported results are from noSMT simulations.

**Table 2: Simulation parameters.**
**(IDQ: Instruction Decode Queue, SB: Store Buffer)**

| | |
|---|---|
| **Basic** | x86-64 core clocked at 3.2 GHz with 2-way SMT support |
| **Fetch & Decode** | 8-wide fetch, TAGE/ITTAGE branch predictors [156], 20-cycle mis-prediction penalty, 32KB 8-way L1-I cache, 4K-entry 8-way micro-op cache, 6-wide decode, 144-entry IDQ, loop-stream detector [41] |
| **Rename** | 6-wide, 288 integer, 220 512-bit and 320 256-bit physical registers, **Memory Renaming [177], zero elimination [68], move elimination [64, 68], constant folding [64, 68], branch folding [60]** |
| **Allocate** | 512-entry ROB, 240-entry LB, 112-entry SB, 248-entry RS |
| **Issue & Retire** | 6-wide issue to 12 execution ports; 5, 3, 2, and 2 ports for ALU, load, store-address, and store-data execution. Port 0, 1, and 5 are used for vector instructions. Aggressive out-of-order load scheduling with memory dependence prediction [51, 120], 6-wide retire |
| **Caches** | **L1-D**: 48KB, 12-way, 5-cycle latency, LRU, PC-based stride prefetcher [69]; **L2**: 2MB, 16-way, 12-cycle round-trip latency, LRU, stride + streamer [47] + SPP [101]; **LLC**: 3MB, 12-way, 50-cycle data round trip latency [15,36], dead-block-aware replacement policy [100], streamer, MESIF [118] protocol |
| **Memory** | 4 channels, 2 ranks/channel, 8 banks/rank, 2KB row-buffer/rank, 64b bus/channel, DDR4, tCAS=22ns, tRCD=22ns, tRP=22ns, tRAS=56ns |
| **Optional** | • **EVES** [155]: exact design of the CVP-1 **32KB** storage track winner<br>• **ELAR** [34]: with additional adder and RSP register in decode stage<br>• **RFP** [164]: 2K-entry prefetch table, 64-entry page address table, 128-entry RFP-inflight table. Total size: **12.5KB**<br>• **Constable** (this work). Total size: **12.4KB** |

### 8.2. Power Modeling

We use an in-house, RTL-validated power model to measure the dynamic power consumption of the core. We report the overall core power consumption by breaking it down into four key units: (1) front end (FE), (2) out-of-order (OOO), (3) non-memory execution unit (EU), and (4) memory execution unit (MEU). We further break down the OOO power into three sub-units: RS, Register Alias Table (RAT), and ROB. We also break down the MEU power into two sub-units: L1-D cache, and data translation look-aside buffer (DTLB). To faithfully model the power consumption of Constable, we estimate the read/write access energy and leakage power of Constable's structures using CACTI 7.0 [31] 22nm library. We scale the estimates to 14nm technology using [171] to make the estimates compatible with our core power model. Table 3 shows the access energy, leakage power, and the area estimate of Constable's structures. We report RMT and SLD power in the RAT component and AMT power in the L1-D component of the core power model.

**Table 3: Access energy, leakage power, and area estimates of Constable's structures in 14nm technology.**

| Component | Read access energy (pJ) | Write access energy (pJ) | Leakage power (mW) | Area (mm2) |
|---|---|---|---|---|
| **SLD** (7.9KB, 3R/2W ports) | 10.76 | 16.70 | 1.02 | 0.211 |
| **RMT** (0.4KB, 2R/6W ports) | 0.15 | 0.20 | 0.31 | 0.004 |
| **AMT** (4.0KB, 1R/1W ports) | 1.58 | 4.22 | 0.74 | 0.017 |

### 8.3. Workloads

We evaluate Constable using 90 workload traces that span across a diverse set of 58 workloads. Our workload suite contains all benchmarks from the SPEC CPU 2017 suite [17], and

many well-known `Client`, `Enterprise`, and `Server` workloads. Each trace contains a snapshot of the processor and the memory state (1) to drive both the functional and microchitecture simulation models, and (2) to faithfully simulate wrong-path execution. Each trace is carefully selected to be representative of the overall workload. Table 4 summarizes the complete list of workloads.

**Table 4: Workloads used for evaluation.**

| Suite | #Workloads | #Traces | Example Workloads |
|-------|-----------|---------|-------------------|
| **Client** | 16 | 22 | DaCapo [3], SYSmark [20], Tablet-Mark [21], JetStream2 [12] |
| **Enterprise** | 9 | 14 | SPECjEnterprise [19], SPECjbb [18], LAMMPS [13] |
| **FSPEC17** | 13 | 29 | All from SPECrate FP 2017 [17] |
| **ISPEC17** | 10 | 11 | All from SPECrate Integer 2017 [17] |
| **Server** | 10 | 14 | Hadoop [1], Linpack [9], Snort [16], Big-Bench [2] |

## 8.4. Evaluated Mechanisms

For a comprehensive analysis, we evaluate Constable standalone and in combination with three prior works: (1) a state-of-the-art load value predictor EVES [155], (2) early load address resolution (ELAR) [34], and (3) register file prefetching (RFP) [164]. For EVES, we use the optimized implementation that won the first championship value prediction (CVP-1) in the 32 KB storage budget track [4]. For ELAR, we follow the same microarchitecture design as proposed in [34]. For RFP, we sweep and select the configuration parameter values that provide the highest performance benefit over the baseline. EVES, RFP, and Constable apply their optimizations to load instructions with data size up to 64 bits. Table 2 shows the overheads of all evaluated mechanisms.

## 8.5. Functional Verification of Constable

Since Constable completely eliminates a load instruction in microarchitectural simulation, we cannot verify the functional correctness of Constable in the same way as LVP or MRN techniques. To functionally verify Constable, we enforce a *golden check* at the retirement stage of every load instruction. The golden check matches the load address and the load data from the functional simulation model with those from the microarchitectural simulation model. In case of a mismatch, the golden check aborts the simulation. We extensively verify the functional correctness of Constable using a broader set of 3400 traces and ensure that no single trace fails the simulation.

## 9. Evaluation

### 9.1. Performance Improvement

**9.1.1. noSMT Configuration.** Fig. 14 shows the geomean performance of EVES, Constable, and Constable and Ideal Constable (§4.4) combined with EVES normalized to the baseline for each workload category. We make three key observations. First, Constable alone improves performance by 5.1% on average over the baseline, which is similar to the performance improvement of EVES (4.7% on average) while incurring $\frac{1}{2} \times$ of EVES' storage overhead. Second, when combined with EVES, Constable improves performance by 8.5% on average over the baseline, which is 3.7% higher than EVES alone. Third, when combined with EVES, Constable provides 82.9% of the performance improvement provided by Ideal Constable.

**Per-workload performance.** To better understand Constable's performance improvement, Fig. 12 shows the performance
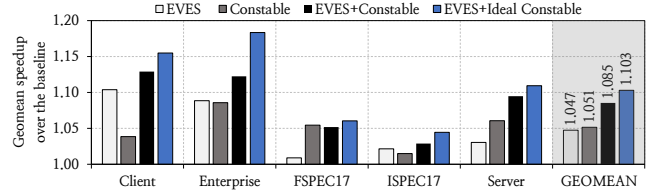


**Figure 11: Speedup over the baseline (noSMT).**

line graph of EVES, Constable, and Constable combined with EVES for every workload. Workloads are sorted in ascending order of the performance gain of EVES over the baseline. We make three key observations. First, Constable outperforms EVES by 4.9% on average in 60 of the 90 workloads (highlighted in green). In the remaining 30 workloads (highlighted in red), EVES outperforms Constable by 9.2% on average. Second, Constable combined with EVES consistently outperforms both EVES and Constable alone in every workload.
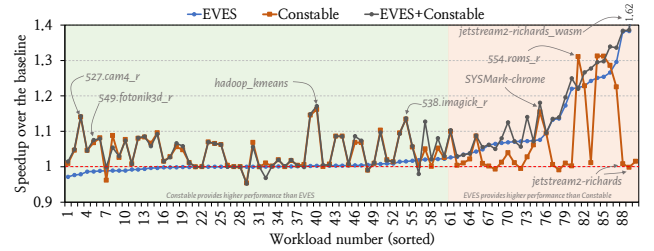


**Figure 12: Speedup of all workloads (noSMT).**

**Load category-wise performance.** To understand the performance benefits contributed by different load categories, Fig. 13 compares the geomean performance of Constable when it eliminates only PC-relative, stack-relative, and register-relative loads with that of a full-blown Constable. The key takeaway is that each three individual types of loads contribute towards Constable's overall performance benefit. Eliminating only PC-relative, stack-relative, and register-relative loads provide a performance improvement of 1.1%, 2.6%, and 1.8%, respectively, which nearly get added up to a 5.1% improvement by the full-blown Constable.
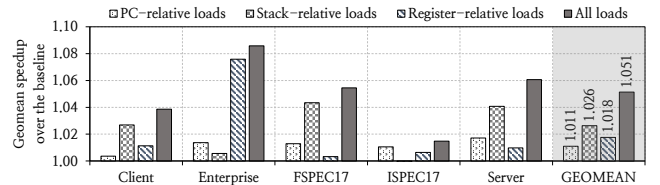


**Figure 13: Speedup of Constable by eliminating execution of only PC-relative, stack-relative, and register-relative loads.**

Based on these results, we conclude that (1) Constable provides a significant performance benefit over a wide range of workloads both by itself and when combined with a state-of-the-art load value predictor EVES, and (2) Constable's performance benefit comes from eliminating all types of loads.

**9.1.2. SMT2 Configuration.** Fig. 14 shows the geomean performance of EVES, Constable, and Constable combined with EVES normalized to the baseline. We make two key observations. First, unlike in noSMT configuration, Constable significantly outperforms EVES in the baseline with SMT2. Constable alone improves performance by 8.8% on average over the base-

line, whereas EVES alone improves performance by 3.6%. This is because, unlike EVES, Constable's load elimination fundamentally reduces utilization of load execution resources, which face increased contention in presence of SMT. Second, combining Constable with EVES continues to provide additional performance benefit than EVES alone. Constable with EVES improves performance by 11.3% on average over the baseline in SMT2. We conclude that Constable provides even more performance benefit in presence of SMT as compared to non-SMT system, due to high resource contention in SMT systems.
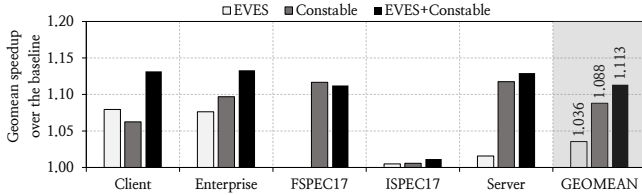


**Figure 14: Speedup over the baseline (SMT2).**

## 9.2. Performance Comparison with Prior Works

Fig. 15 shows the geomean performance of Constable standalone and when combined with ELAR and RFP in the baseline. We make two key observations. First, Constable alone outperforms both ELAR and RFP. ELAR, RFP, and Constable improve performance on average by 0.74%, 4.4% and 5.1%, respectively over the baseline. ELAR provides relatively small performance benefit over baseline as our baseline already implements constant folding [64,68], which can track stack register modifications in the form of $RSP \leftarrow RSP \pm immediate$ before the execution stage. Second, when combined with ELAR and RFP, Constable provides more performance benefit than ELAR and RFP alone, respectively. This shows that Constable can be applied along with these proposals to provide even more performance benefit.
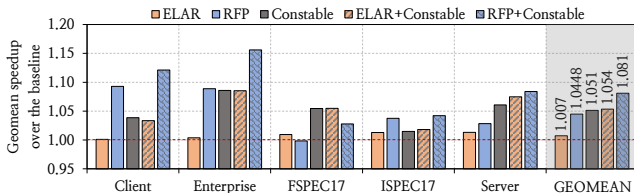


**Figure 15: Speedup of Constable over ELAR and RFP.**

## 9.3. Loads Eliminated by Constable

Fig. 16 shows the load coverage (i.e., the fraction of load instructions that are either eliminated or value-predicted by Constable or EVES, respectively) of EVES, Constable, and Constable and Ideal Constable combined with EVES in the baseline system. We make three key observations. First, Constable alone covers 23.5% of the loads, whereas EVES covers 27.3%. This is because Constable target loads which show *both* value and address locality (i.e., repeatedly fetching same value from same memory address), whereas EVES target loads that show only value locality. Despite its lower coverage, Constable matches performance of EVES as Constable mitigates *both* data dependence and resource dependence on covered loads. Second, Constable combined with EVES has higher load coverage (35.5% on average) than EVES alone. Third, when combined with EVES, Constable provides 85.4% of the coverage of Ideal Con-

stable. We conclude that Constable covers a significant fraction of the load instructions both by itself and combined with EVES.
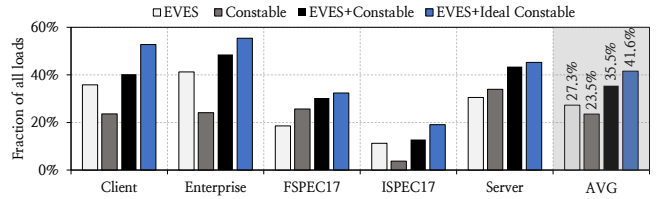


**Figure 16: Load coverage of Constable versus EVES.**

**9.3.1. Coverage of Global-Stable Loads.** To understand Constable's coverage of global-stable loads (see §4), Fig. 17 shows the breakdown of loads in each addressing-mode category into three classes: (1) loads that are global-stable and eliminated by Constable, (2) loads that are global-stable but not eliminated, and (3) loads that are not global-stable but eliminated. We make three key observations. First, PC-relative and register-relative global-stable loads see the highest and the lowest runtime elimination coverage of 70.2% and 33.2%, respectively. Second, Constable successfully eliminates 56.4% of all global-stable loads on average at runtime. For the remaining 43.6% global-stable loads, Constable misses their elimination opportunity due to three key reasons (not shown in the figure): (a) at least one source architectural register of a global-stable load instruction gets written between its two successive dynamic instances (for 23.3% of all global-stable loads), (b) a *silent store* [35,104–106] occurs between two successive dynamic instances of a global-stable load (for 14.1% of all global-stable loads), and (c) coverage loss due to other reasons, e.g., stability confidence learning and limited hardware budget for likely-stable load tracking (for 6.2% of all global-stable loads). Third, on average, 13.5% more loads are eliminated by Constable at runtime which are not identified as global-stable. This is because these loads are not stable across the entire workload trace, but stable in a workload phase to meet the stability confidence threshold and and hence get eligible for elimination. Based on these results, we conclude that Constable eliminates a significant fraction of the global-stable loads at runtime. However many elimination opportunities are still left, which can be unlocked by future works to achieve even higher performance and power efficiency improvements.
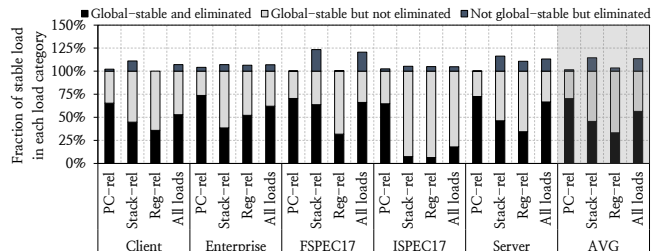


**Figure 17: Breakdown of eliminated and non-eliminated loads as a fraction of global-stable loads.**

## 9.4. Impact on Pipeline Resource Utilization

**9.4.1. Reduction in RS Allocation.** Fig. 18(a) plots the percentage reduction in RS allocations in a system with Constable over the baseline system as a box-and-whiskers plot. The key observation is that Constable reduces the RS allocation by 8.8% on average (up to 35.1%) across all workloads. `Server`

and `ISPEC17` workloads experience the highest and the lowest average RS allocation reductions of 12.8% and 1.3%, respectively. 37 of the 90 workloads experience a reduction in RS allocation by more than 10%.
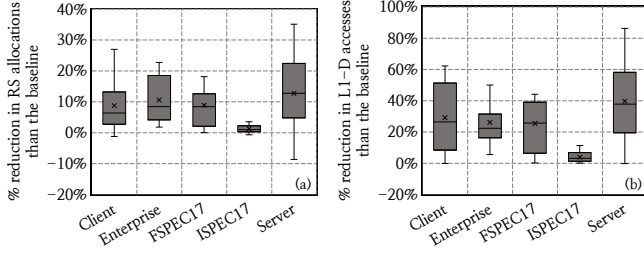


Figure 18: Reduction in (a) RS allocations and (b) L1-D accesses.

**9.4.2. Reduction in L1-D Access.** Fig. 18(b) plots the percentage reduction in L1-D accesses in a system with Constable over the baseline as a box-and-whiskers plot. The key observation is that Constable reduces L1-D allocation by 26.0% on average. Similar to the reduction in RS allocation, `Server` and `ISPEC17` workloads experience the highest and the lowest average L1-D access reduction of 39.7% and 3.9%.

Based on these results, we conclude that, by eliminating load execution, Constable significantly reduces RS allocations and L1-D accesses, both of which aid in improving performance (§9.1) and reducing dynamic power consumption (§9.5).

## 9.5. Power Improvement

Fig. 19(a) shows the core power consumption (and its breakdown) in a system with EVES, Constable, and EVES+Constable normalized to the baseline. The key takeaway is that Constable reduces the core power consumption by 3.4% on average over the baseline, whereas EVES reduces power by only 0.2%. This is because, unlike EVES where the value-predicted load instructions get executed nonetheless, Constable eliminates executing likely-stable loads altogether. To understand the distribution of the power benefit across various core structures, we further expand the power consumption of OOO and MEU units in Fig. 19(b) and (c) respectively. As Fig. 19(b) shows, Constable reduces the power consumed by OOO unit by 4.5% on average over the baseline. The RS sub-unit of OOO unit experiences the highest power reduction of 5.1% (marked by braces). This is because Constable significantly reduces the number of RS allocations (§9.4.1). As Fig. 19(c) shows, Constable also reduces the power consumed by MEU unit by 7.2% on average over the baseline. The MEU power reduction is dominated by L1-D cache, which experiences 9.1% reduction in power (marked by braces) on average. This is largely due to the reduction is L1-D accesses (§9.4.2). We conclude that Constable, unlike value prediction, reduces the core power by fundamentally eliminating load execution.

## 10. Other Related Works

**Compiler-based optimizations** like global value numbering [56, 150], common subexpression elimination [57], and loop-invariant code motion [81] identify pieces of code that stay invariant across various granularities of a program and eliminate their redundant execution. All the workloads used in this work are already compiled with these optimizations. We demonstrate that Constable provides performance benefits on top of such well-optimized workloads.
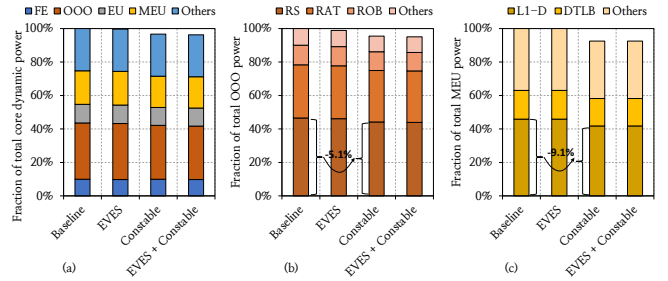


Figure 19: (a) Overall core power consumption normalized to baseline. Expanded view of (b) OOO power and (c) MEU power.

**Data caching** [75, 109, 182] reduces the average memory access latency by storing the data that would likely get accessed in the near future in faster on-chip memory. Prior works have proposed techniques to improve cache hit-rate by (1) exploiting data reuse patterns (e.g., [88–90, 132, 145, 157, 183]), (2) predicting dead cachelines (e.g., [93, 100, 175]), and (3) applying machine learning techniques(e.g., [111, 112, 162]). Constable can be orthogonally combined with caching techniques. Our baseline system employs a dead-block-aware replacement policy in the LLC (Table 2).

A **data prefetcher** predicts the address of future memory requests and fetches the data from slower memory to faster on-chip caches before the program demands it. A prefetch request can be generated by software [24, 25, 44, 113, 188] or hardware. Hardware prefetchers can generate prefetch request by (1) pre-executing program code [61, 77, 78, 84, 122–130], (2) learning memory access pattern over spatial memory regions [28, 30, 37, 38, 40, 47, 69, 85, 91, 92, 96, 101–103, 110, 115, 131, 135, 144, 158, 161, 169, 170], and (3) memorizing long sequences of past demanded memory addresses [29, 33, 49, 50, 59, 65, 82, 87, 95, 99, 163, 168, 179–181, 184, 185]. Constable can be orthogonally applied with any prefetcher. Our baseline system employs multiple data prefetchers across the cache hierarchy (Table 2).

## 11. Conclusion

We introduce Constable, a purely-microarchitectural technique that safely eliminates the execution of load instructions while breaking the load data dependence. Our extensive evaluation using a wide range of workloads and system configurations shows that Constable provides significant performance benefit and reduced dynamic power consumption by eliminating load execution. As hardware resource scaling becomes challenging in future processors, we believe and hope that Constable's key observations and insights would inspire future works to explore a multitude of other optimizations that mitigates ILP loss due to resource dependence and load instruction execution.

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# A. Extended Evaluation

## A.1. Performance Sensitivity

### A.1.1. Sensitivity to Load Execution Width Scaling.
Fig. 20(a) shows the geomean speedup of Constable and the baseline system over the baseline configuration when we increase the load execution width (i.e., increasing both number of AGU and load ports). We make two key observations. First, Constable *consistently* adds performance on top of the baseline system even if we naively scale the load execution width. With increasing AGU and load ports (while keeping the pipeline depth resources same), the resource dependence stemming from load reduces. Yet, Constable outperforms the baseline system by $3.5\%$ with $2\times$ load execution width than the baseline configuration. Second, adding Constable on the baseline system configuration (i.e., with 3 load execution width) essentially provides the similar performance benefit as the baseline system with one extra load execution width, while incurring lower area overhead and *reducing* power consumption.
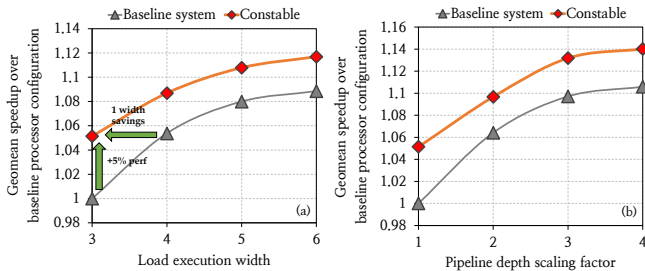


**Figure 20: Performance sensitivity to (a) load execution width, and (b) pipeline depth.**

### A.1.2. Sensitivity to Pipeline Depth Scaling.
Fig. 20(a) shows the geomean speedup of Constable and the baseline system over the baseline configuration when we scale pipeline depth resources (i.e., size of ROB, RS, LB and SB). The key takeaway is that Constable *consistently* adds performance on top of the baseline system even if we naively scale the pipeline depth. With $4\times$ depth scaling, Constable improves performance of the baseline system by $3.4\%$ on average.

## A.2. Effect of Eliminated Load Disambiguation with In-Flight Stores

When the computed address of an in-flight store instruction matches with that of an eliminated load younger than the store, the existing memory disambiguation logic catches such memory ordering violation and re-executes all instructions younger than (and including) the incorrectly-eliminated load (see §6.5). Thus a frequent memory ordering violation by eliminated loads may incur a significant performance and power overhead on Constable. To understand such overhead, we show the fraction of loads eliminated by Constable that violate memory ordering as a box-and-whiskers plot in Fig. 21(a). As we can see, an eliminated load rarely violates memory ordering. On average, only $0.09\%$ of all eliminated loads violate memory ordering. Less than $0.5\%$ of eliminated loads violate memory ordering in 86 out of 90 workloads. This is primarily due to Constable's confidence-based mechanism that considers a load instruction eligible for elimination only if it meets a sufficiently-high stability confidence level threshold (set to 30 in our evaluation). Fig. 21(b) further shows the increase in instructions allocated to the ROB in presence of Constable as compared to the baseline

system to understand the effect of such rare memory ordering violations. As we can see, Constable increases the allocated instructions by only $0.3\%$ on average across all workloads. 79 out of 90 workloads observe an increase of less than $1\%$.

Thus, we conclude that Constable observes a very insignificant overhead due to rare memory ordering violations by incorrectly-eliminated loads.
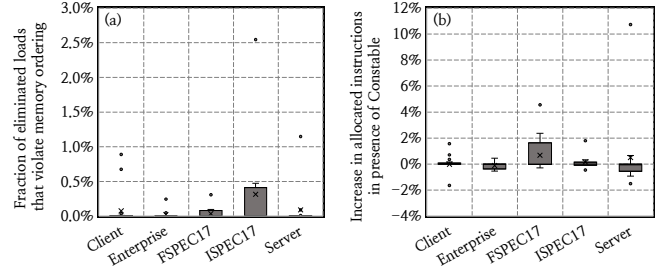


**Figure 21: (a) Fraction of loads eliminated by Constable that violate memory ordering. (2) Increase in instructions allocated to ROB in presence of Constable.**

## A.3. Effect of Loss of Elimination Opportunities due to Clean Evictions

In order to correctly eliminate load instructions in a multi-core system, Constable proposes pinning the CV-bit of a cacheline that is accessed by an eliminated load instruction (see §6.6). However, the change in the coherence protocol may complicate hardware verification. Another alternative design could be to avoid elimination on every core-private cache eviction. However, this design choice may lose elimination opportunities if the evicted cacheline is clean. In this section, we quantify impact of such elimination opportunity loss on Constable's performance and elimination coverage.

To understand the effect, we model a Constable variant that looks up AMT for every L1 data (L1-D) cache eviction and invalidates the AMT entry. This prevents Constable from eliminating any further load instructions that access the evicted cacheline. We call this Constable variant Constable-AMT-I. Fig. 22(a) compares the speedup of Constable-AMT-I with the vanilla Constable. Constable-AMT-I loses $0.9\%$ performance improvement than the vanilla Constable on average across all workloads. 11 out of 90 workloads observe a performance loss of more than $5\%$ in Constable-AMT-I (with the highest performance loss of $10.4\%$ in 554.roms_r) as compared to vanilla Constable. The performance loss is primarily attributed to the loss in elimination coverage. As Fig. 22(b) shows, Constable-AMT-I provides $3.4\%$ less load elimination coverage than the vanilla Constable. 17 out of 90 workloads observe a coverage loss of more than $5\%$ in Constable-AMT-I (with the highest coverage loss of $27\%$ in 554.roms_r). Thus, we conclude that CV-bit pinning is a more-performant design choice than avoiding elimination on every core-private cache eviction.

## B. Effect of Increasing Architectural Registers on Global-Stable Loads

Increasing architectural registers enables a compiler to exploit additional registers to capture data reuse, which otherwise would have been reused via memory. Thus increasing architectural registers typically reduces the number of load and store instructions in a program. To understand the effect of increasing architectural registers on global-stable load instructions,
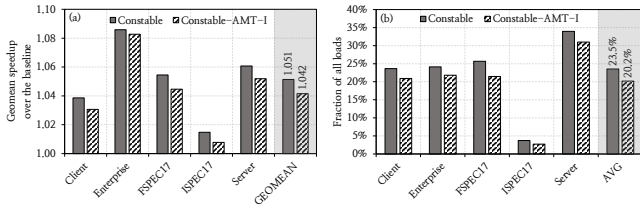
**Figure 22: (a) Speedup and (b) coverage of Constable with AMT invalidation on L1D eviction compared to a vanilla Constable.**

we compile all C/C++-based workloads from SPEC CPU 2017 rate suite [17] without and with Intel APX extension [11], that doubles the number of architectural registers in x86-64 ISA from 16 to 32, using Clang 18.1.3 [14]. We run these workloads using the test input and profile their *end-to-end execution* using the Load Inspector tool (see §4.1) to observe (1) the reduction in dynamic loads caused by APX, and (2) the fraction of all dynamic loads that are global-stable in workloads without and with APX.

Fig. 23 shows the fraction of all dynamic loads that are global-stable in each workload without and with APX (as bar graph on the left y-axis) and the reduction in dynamic loads with APX extension (as markers on the right y-axis) for all C/C++-based workloads from SPEC CPU 2017 suite.[11]
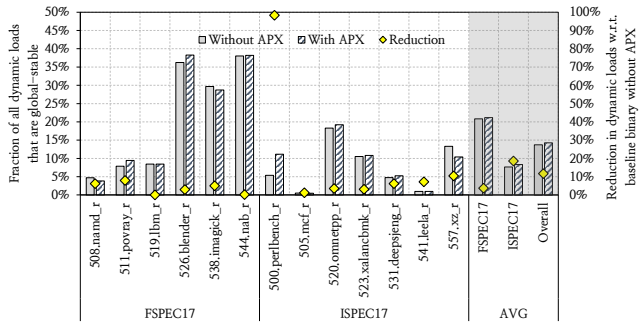


**Figure 23: Fraction of all dynamic loads that are global-stable in workloads compiled without and with APX (on the left y-axis) and the reduction in dynamic loads by APX (on the right y-axis).**

We make two key observations from Fig. 23. First, the fraction of dynamic loads that are global-stable (i.e., the elimination opportunities for Constable) is much higher than the reduction in dynamic loads by doubling the number of architectural registers. APX reduces the number of dynamic loads by 11.7% on average. `500.perlbench_r` is an outlier that observes a reduction of 98.3% of loads. Without it, APX reduces the dynamic loads by only 4.5% on average. On the other hand, 13.7% and 14.2% of all dynamic loads on average are global-stable in workloads without and with APX, respectively.[12] The difference is more prominent for `FSPEC17` workloads, where APX reduces dynamic loads by only 3.7%, whereas 20.8% and 21.2% of dynamic loads are global-stable in without and with APX, respectively. Second, the fraction of dynamic loads that are global-stable is nearly the same in workloads without and with APX. `500.perlbench_r` and `557.xz_r` are only two

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[11] `502.gcc_r`, `510.parest_r` and `525.x264_r` are omitted from this study due to failed compilation using Clang.

[12] Note that, the global-stable load fraction reported here is slightly lower than that reported in Fig. 3(a). This is because, the earlier study in Fig. 3(a) uses the representative sections of the workloads (see §8.3) to limit the simulation overhead, while this study instruments each workload *end-to-end*.

workloads that show more than 3% absolute change in the global-stable load fraction. This shows that the elimination opportunities for Constable is largely orthogonal to the benefits of increasing architectural registers.

To further analyze the change in characteristics of global-stable loads in presence of APX, we break down the global-stable loads based on their addressing modes in workloads both without and with APX in Fig. 24. We make two key observations from this figure. First, the fraction of stack-relative global-stable loads reduces in presence of APX. On average, 21.1% and 16% of all global-stable loads use stack-relative addressing in workloads without and with APX, respectively. This is expected, since increasing architectural registers predominantly reduces stack loads. Second, the fraction of PC-relative global-stable loads stays nearly the same in presence of APX (38.3% without APX as compared to 38.9% with APX). This shows that doubling architectural registers alone cannot eliminate all memory accesses to global-scope variables which are effectively runtime constant.
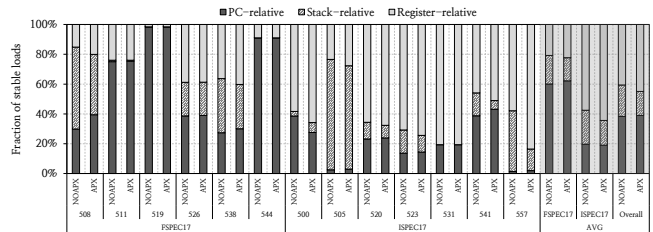


**Figure 24: Distribution of global-stable loads by their addressing modes in workloads without and with APX. Each number on the x-axis corresponds to the respective workload from SPEC CPU 2017 suite.**

Based on these results, we conclude that the two load elimination techniques - at compile time by increasing architectural registers and at runtime by Constable - are largely *orthogonal* to each other. Thus, Constable would likely be equally-performant and power-efficient in presence of increased architectural registers, as it is with the current set of architectural registers.